applying a first voltage pulse with a first polarity to a memory cell top electrode;

in response to the first voltage pulse, creating a low resistance in an asymmetrical-area colossal magnetoresistance (CMR) memory film;

applying a second voltage pulse with a second polarity, opposite of the first polarity, to the memory cell top electrode; and,

in response to the second voltage pulse, creating a high resistance in the asymmetric-area CMR memory film;

applying a third pulse, having the same polarity as the second voltage pulse, and a pulse width of greater than 1 microsecond; and,

in response to the third pulse, creating a low resistance in the CMR memory film.

[[15]] 16. (currently amended) The method of claim [[14]] 15 wherein creating a low resistance in the CMR memory film in response to the first pulse includes creating a low resistance in a narrow-area region of the asymmetric-area CMR memory film; and,

wherein creating a high resistance in the CMR memory film in response to the second pulse includes creating a high resistance in the narrow-area region of the asymmetric-area CMR memory film.

[[16]] 17. (currently amended) The method of claim [[15]] 16 wherein creating a low resistance in the CMR memory film in response to the first pulse includes creating a resistance in the range of 1000 to 10k ohms; and,

field, with a field intensity less than the first field, in a wide-area region of the CMR memory film; and,

wherein includes creating a high resistance in a narrow-area region of the asymmetric-area CMR memory film in response to the second pulse includes creating a high resistance in response to a third electric field in the narrow-area region of the CMR memory film, opposite in polarity to the first field, and a fourth electric field, with a field intensity less than the third field, in a wide-area region of the CMR memory film.

[[20]] 21. (currently amended) The method of claim [[15]] 16 wherein applying [[a]] the first pulse with [[a]] the first polarity to the memory cell top electrode includes applying a positive polarity pulse;

wherein creating a low resistance in a narrow-area region of the asymmetric-area CMR memory film includes creating a low resistance in a narrow-area region adjacent the top electrode;

wherein applying [[a]] the second pulse with [[a]] the second polarity to the memory cell top electrode includes applying a negative polarity pulse; and,

wherein creating a high resistance in a narrow-area region of the asymmetric-area CMR memory film includes creating a high resistance in a narrow-area region adjacent the top electrode.

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~~21~~-34. Canceled